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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,651	12/30/2003	Chih-Wei Wu	12392-US-PA	1650

31561 7590 03/23/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,651	WU, CHIH-WEI	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Do, US Patent no. 6,367,007.

Regarding claim 1, AAPA discloses a method for updating a BIOS, comprising:

performing a power-on self test by a data processing device [element 100 in Figure 2a];

the data processing device checking a keyboard status and performing specific key-in commands [element 110 in Figure 2a];

detecting a memory and a setting status of said memory by said data processing device [element 120 in Figure 2a];

detecting peripheral devices of said data processing device and a setting status of said peripheral devices [element 130 in Figure 2a];

determining whether to enter into a setup menu of said BIOS [element 140 in Figure 2a];

displaying a user interface of said setup menu [element 150 in Figure 2a];

determining whether to exit from said setup menu [element 160 in Figure 2a];

confirming whether to save a change of BIOS settings [element 170 in Figure 2a]; and

saving said change of said BIOS settings into a CMOS [element 110 in Figure 2a].

AAPA does not disclose providing a memory to store at least one set of system configuration settings, determining whether said set of system configuration settings is triggered and performing functions of said system configuration settings. Do discloses providing a memory to store at least one set of system configuration settings [Flash ROM, column 1, lines 52-55], determining whether said set of system configuration settings is triggered [determining whether optional components are installed in the computer, column 1, lines 60-65] and performing functions of said system configuration settings [executing custom program code, column 2, lines 14-19]. It would have been obvious to one of ordinary skill in the art to modify the AAPA method to provide a memory to store at least one set of system configuration settings. Providing a separate memory to store system configuration settings allows for more custom system configurations to be supported by the BIOS [Do, column 1, lines 52-56].

Regarding claim 5, AAPA and Do disclose that the data processing device is a desktop computer [Do, column 1, lines 12-13].

Regarding claim 10, AAPA discloses a method for updating a BIOS to simplify change of a setting for said BIOS, said method comprising:

performing a power-on self test by a data processing device [element 100 in Figure 2a];

the data processing device checking a keyboard status and performing specific key-in commands [element 110 in Figure 2a];

detecting a memory and a setting status of said memory by said data processing device [element 120 in Figure 2a];

detecting peripheral devices of said data processing device and a setting status of said peripheral devices [element 130 in Figure 2a];

AAPA does not disclose providing a memory to store at least one set of system configuration settings, determining which one of said set of system configuration settings is triggered and performing functions of said system configuration settings. Do discloses providing a memory to store at least one set of system configuration settings [Flash ROM, column 1, lines 52-55], determining which one of said set of system configuration settings is triggered [determining whether optional components are installed in the computer, column 1, lines 60-65] and performing functions of said system configuration settings [executing custom program code, column 2, lines 14-19]. It would have been obvious to one of ordinary skill in the art to modify the AAPA method to provide a memory to store at least one set of system configuration settings. Providing a separate memory to store system configuration settings allows for more custom system configurations to be supported by the BIOS [Do, column 1, lines 52-56].

Regarding claim 14, AAPA and Do disclose that the data processing device is a desktop computer [Do, column 1, lines 12-13].

Claims 2-4, 6-9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Do, US Patent no. 6,367,007, in view of Christeson, US Patent no. 5,822,581.

Regarding claims 2-4 and 11-13, AAPA and Do, as described above, disclose a method for updating a BIOS. AAPA and Do, do not disclose a reset mode, including resetting data in the CMOS and a writing mode, including writing data stored in a backup memory into the CMOS. However, as shown by Christeson, resetting a CMOS or writing backup data into a CMOS is well known in the art. Christeson discloses a reset mode, including resetting data in the CMOS

[LOAD CMOS WITH BIOS DEFAULTS in Figure 5] and a writing mode, including writing data stored in a backup memory into the CMOS [RESTORE CMOS FROM FLASH BACKUP in Figure 5]. It would have been obvious to one of ordinary skill in the art to include the well known CMOS reset and write modes into the AAPA and Do method in order to restore computer system operation in the case that the CMOS has been corrupted.

Regarding claims 6-9, AAPA and Do, as described above, disclose a method for updating a BIOS. AAPA and Do, do not disclose a backup mode, including writing CMOS data into a backup memory, a loading mode, including writing data in backup memory into a CMOS and a rename mode, including renaming an item displayed a setup menu. However, a backup mode, a loading mode and a renaming mode are all well known in the art. Christeson discloses a backup mode, including writing CMOS data into a backup memory [SAVE CURRENT CMOS IMAGE TO FLASH in Figure 4], a loading mode, including writing data in backup memory into a CMOS [RESTORE CMOS FROM FLASH IMAGE in Figure 4] and a rename mode, including renaming an item displayed a setup menu [user programs custom configuration information, column 6, lines 2-5]. It would have been obvious to one of ordinary skill in the art to include the well known CMOS backup, loading and renaming modes into the AAPA and Do method in order to allow a user to customize configuration information and to allow the user to restore computer system operation in the case that the CMOS has been corrupted.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stevens, US Patent no. 6,633,976, discloses storing BIOS modules on a secondary nonvolatile storage.

Christeson, US Patent no. 6,622,243, discloses backing up and loading configuration information from a CMOS memory to non-volatile memory.

Kao et al., US Patent no. 6,119,192, discloses storing initialization information in a supplemental EEPROM separate from the conventional system BIOS.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Paul Yanchus
March 15, 2006